MOTOROLA

STATION CONTROL MODULE

MODEL CLN1201

1 DESCRIPTION

The CLN1201 Station Control Module (SCM) is described in this section. A general description, identification of controls, indicators, and inputs/outputs, a functional block diagram, and functional theory of operation are provided. The information provided is sufficient to give service personnel a functional understanding of the module, allowing maintenance and troubleshooting to the module level. (Refer also to the Maintenance and Troubleshooting section of this manual for detailed troubleshooting procedures for all modules in the station.)

General Description

The SCM serves as the main controller of the station. The SCM contains an MC68356 microprocessor which forms the heart of the module. This IC combines a 68302 Integrated Multiprotocol Processor (IMP) with a 56002 Digital Signal Processor (DSP) which, along with the support circuitry, provides signal processing and operational control over the other station modules.

The CLN1201 provides for Motorola Radio-Telephone Interconnect (MRTI) and 6809 trunking capabilities. In addition, the CLN1201 provides a Receiver Signal Strength Indication (RSSI) output and an external reference input for connection to a high stability oscillator.

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Overview of Circuitry

The SCM contains the following circuitry:

- Host Microprocessor – that part of the MC68356 which serves as the central controller for the station and the SCM
- Non-Volatile Memory – consists of Flash EPROM memory, containing both the system operating software and the station codeplug data
- SRAM Memory – Static RAM serves as short term storage for data
- Digital Signal Processing (DSP) and DSP ASIC Circuitry – that part of the MC68356 (and associated ASIC) which performs high-speed processing of all audio and signalling data signals
- Station Reference Circuitry – generates the 2.1 MHz reference signal used throughout the station
- Serial Peripheral Interface (SPI) Input / Output Circuitry – provides high-speed serial bus to pass control and diagnostic information between the Host microprocessor, the station modules (receiver, exciter, PA, etc.) and various serially-controlled devices on the SCM
- Serial Input / Output Circuitry – provides bus circuitry to buffer two of the Host microprocessor Serial Communication Interface (SCI) ports (SCC1 and SCC2) for communication with optional modules, and an external IBM-PC running Radio Service Software (RSS)
- Audio Processing Circuitry – routes the various audio input signals (such as microphone, wireline, and receiver audio) to output devices (such as external speaker and exciter modulation inputs) and converts (via various codecs) the audio signals between digital and analog formats for serial transmission to / from the DSP
- Parallel I / O Circuitry – provides the necessary logic interface for the Host microprocessor to send / receive miscellaneous control signals to / from various station modules and externally connected equipment, and to control the status LEDs on the front panel
- Supply Voltage Circuitry – contains filtering, voltage doubling and regulatory circuitry which accepts various input voltages from backplane regulators and the power supply, and generates the operating voltages required by the Receiver and Exciter modules, and the SCM

2 INDICATORS AND INPUT/OUTPUT CONNECTIONS

Figure 1 shows the SCM indicators, and all input and output external connections.

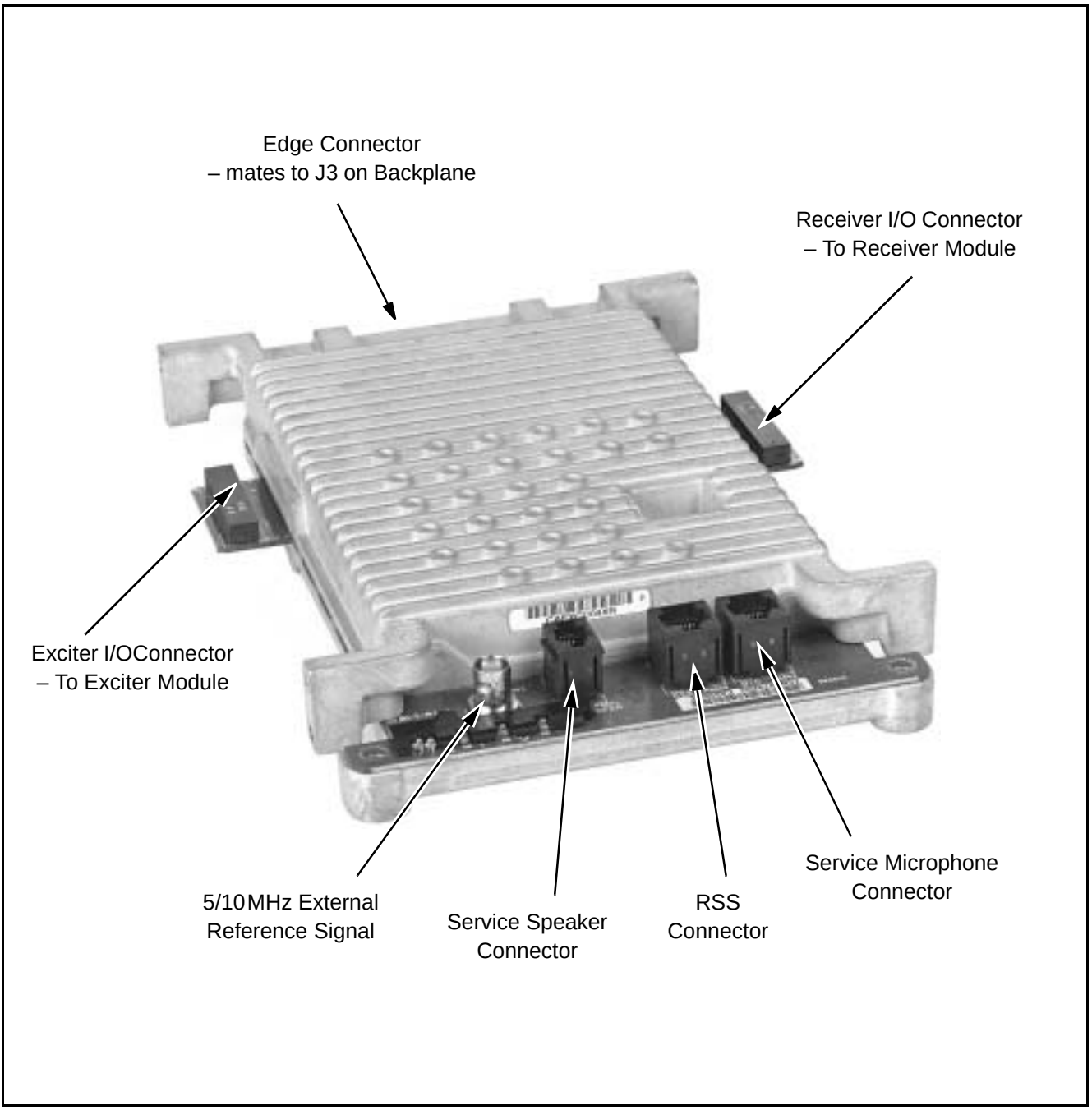


Figure 1. Station Control Module Indicators and Input/Output Connections

3 FUNCTIONAL THEORY OF OPERATION

The following theory of operation describes the operation of the SCM at a functional level. The information is presented to give the service technician a basic understanding of the functions performed by the module in order to facilitate maintenance and troubleshooting to the module level. Refer to Figure 2 for a block diagram of the SCM supply voltage circuitry. Refer to Figure 3 for a block diagram of the other sections of the SCM circuitry.

Host Microprocessor

General

The SCM utilizes an MC68356 Microprocessor which combines microprocessor and DSP capabilities on a single device. The Host Microprocessor (µP) functions of the SCM are performed by an MC68302 Integrated Multiprotocol Processor (IMP) which is one part of the MC68356. This part serves as the main controller for the SCM (and station), controlling the operation of the station as determined by the station software and codeplug (both stored in a non-volatile Flash EPROM device).

The µP is equipped with a 23-line address bus; only 18 lines are required to access the non-volatile Flash memory, SRAM memory, and provide control (via memory mapping) for Parallel I/O circuitry in the SCM. The Host µP operates in MC68008 mode, providing an 8-bit data bus which (buffered for the Flash and SRAM memory) is used to transfer data to/from the SCM memory, as well as Parallel I/O circuitry. The Host µP also provides the signals controlling the demultiplexers used to route various audio inputs/outputs in the Audio Processing circuitry of the SCM.

Station Software/Codeplug Flash Memory

The station control software and the data which determines the station personality (i.e. codeplug) both reside in one 1 MB x 8 Flash EPROM. This device is accessed by the Host µP via the Host Address Bus and the (buffered) 8-line Host Master Data Bus.

Stations are shipped from the factory with generic default data programmed into the codeplug portion of the Flash. Field programming is performed during installation using the RSS to enter additional customer-specific data, such as site output power, time-out timer settings, etc.

SRAM Memory

Each SCM contains 256 Kbyte of SRAM which provides short-term storage for data generated/required during normal operation.

Host µP Clock Generation

The Host µP operates at a 20.4 MHz rate, generated internally from a reference clock. A high-stability VCO in the Station Reference circuitry generates the station master clock (16.8 MHz) which is divided by 14 (in the DSP ASIC) to 1.2 MHz and routed to the EXTAL pin of the Host µP. The Host µP multiplies this reference (under software control) by 17 to produce an internal system clock of 20.4 MHz.

Address Decoding

Host µP read and write operations are performed using the Host Address and Data buses in conjunction with four programmable chip select lines from the internal MC68356 chip select generators, CS0 to CS3, which are used in the following manner.

- CS0 is used to control access to the Flash (EPROM) memory space. Since the Flash device stores station control software, CS0 is also enabled after a reset to access the boot ROM upon system start-up.
- CS1, CS2 are used to control access of up to two SRAM devices.
- CS3 is used to control access to the Parallel I/O circuitry (control signals and SPI bus chip selects for station modules and external options).

Serial I/O Circuitry

The Serial I/O circuitry interfaces with two of the Serial Communications Interface (SCI) ports (SCC1 and SCC2) on the Host µP to provide general-purpose serial communications buses, as follows:

- SCC1 – this port is buffered to provide a high-speed Interprocessor Communications Bus, allowing the Host µP to communicate with optional modules (via the backplane)
- SCC2 – serves as a serial RSS port. An 8-pin Telco connector is provided on the front of the SCM to allow service personnel to connect a PC loaded with the Radio Service Software (RSS) to the station, and perform programming and maintenance tasks. EIA-232 Bus Receivers/Drivers interface the connector to the SCC2 port.

SPI I/O Circuitry

The Serial Peripheral Interface (SPI) I/O circuitry provides a SPI bus which is used as a general-purpose communications bus to allow the Host µP to communicate with other modules in the station. The SPI I/O circuitry also includes an A/D converter which allows the Host µP to determine (via the SPI bus) the connected optional modules and other station characteristics.

The SCM is always configured as the SPI bus master, while other modules (Receiver, Exciter, PA, etc.) are configured as bus slaves. Two slave configurations are possible:

- Basic slave – these are SPI-compatible ICs, located on the slave modules (e.g., A/D and D/A converters, and frequency synthesizers).
- Intelligent slave – these are slave modules which contain a microprocessor having a local SPI bus (e.g., intelligent equipment connected to the station via the Systems connector on the backplane).

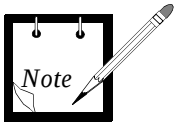
There are three SPI signals, as follows:

- SPI CLK – derived from the internal Host µP clock. With a Host µP clock frequency of 20.4 MHz, the minimum SPI CLK is approximately 319 KHz. It is used to shift serial data from the Host µP to a slave, and from the slave back to the Host µP.
- MOSI (Master Out Slave In) – provides the data path containing information from the master (SCM) to the slave (Receiver, Exciter, PA, etc.). This is an output from the Host µP.
- MISO (Master In Slave Out) – provides the data path containing information from the slave to the master. This is an input to the Host µP.

Station Reference Circuitry

The Station Reference Circuitry incorporates a high-stability VCO ("pendulum" IC) to generate a stable 16.8 MHz signal which is fed to the DSP ASIC. The ASIC divides the signal by 8 and outputs a 2.1 MHz signal which is buffered and filtered by a splitter and output to the Exciter Module and Receiver Module as 2.1 MHz REF.

The CLN1201 SCM includes a phase-locked loop (PLL) IC. Higher stability is achieved by phase-locking the pendulum IC to a 5/10 MHz external reference source from an external high-stability oscillator, allowing the pendulum IC to be automatically adjusted to this source (referred to as "auto-netting").



A BNC connector (located on the front of the CLN1201) is provided to allow the highly-stable external 5 / 10 MHz source to be input to the OSC_{IN} input of the PLL to perform frequency netting. Refer to the Routine Maintenance section in this manual for recommended intervals and procedures for netting the station reference.

The Station Reference Circuitry may operate in one of three modes:

- Normal Mode – In this mode, the control voltage is turned off (via control voltage enable switch) and the high-stability VCO operates in an open loop mode; stability of the VCO in this mode is 2 PPM per year.
- Manual Netting Mode – Periodically, an external 5 / 10 MHz source is required to fine tune, or "net", the 16.8 MHz reference signal. In this mode, the PLL compares the 5 / 10 MHz reference and a sample of the 16.8 MHz VCO output and generates up / down pulses. The Host µP reads the pulses (via SPI bus) and sends correction signals (via SPI bus) to the VCO to adjust the output frequency to 16.8 Mhz ±0.3 ppm.
- High-Stability Mode – For some systems, the free-running stability of the VCO is unacceptable for optimum system performance. Therefore, an external 5 / 10 MHz source is connected permanently to the BNC connector. In this mode, the PLL compares the 5 / 10 MHz reference and a sample of the 16.8 MHz VCO output and generates a dc correction voltage. The control voltage enable switch is closed, allowing the control voltage from the PLL to adjust the high-stability VCO frequency to 16.8 Mhz ±0.3 ppm. The VCO operates in this closed loop mode and is continually being frequency-controlled by the control voltage from the PLL.

Digital Signal Processor (DSP) and DSP ASIC Circuitry

General

The second half of the MC68356 contains a 56002 Digital Signal Processor (DSP). All station transmit and receive audio / data is processed by the DSP and related circuitry. This circuitry includes the DSP, the DSP ASIC, and the Audio Processing circuitry. All audio signals input to or output from the DSP ASIC are in digitized format. The digitized audio is transfered to / from various codec ICs in the Audio Processing circuitry along corresponding serial buses (dependent on the particular routing of an audio signal).

Inputs to the DSP circuitry are:

- Digitized receive signals from the Receiver Module
- Audio from handset or microphone connected to appropriate SCM connector (behind the station front panel)
- Digitized voice audio / data from Wireline Interface Board via PCM Codec Bus
- Auxiliary TX Audio from Systems connector on backplane
- MRTI TX Audio from Trunking / MRTI connector on backplane
- Trunk TX Data from Trunking / MRTI connector on backplane

Outputs from the DSP circuitry are:

- Digitized voice audio / data from DSP to Wireline Interface Board via PCM Codec Bus
- Digitized voice audio / data from DSP to Exciter Module (modulation signals) via Audio Processing circuitry
- Digitized voice audio from DSP to external speaker via Audio Processing circuitry; speaker is connected to appropriate SCM connector behind the station front panel
- Trunk RX Audio (voice and control channel) to Trunking / MRTI connector on backplane
- MRTI RX Audio to Trunking / MRTI connector on backplane

Digital Signal Processor (DSP)

The DSP operates at a clock speed of 60 MHz with no wait states. The DSP accepts and transmits digitized audio to / from the various modules in the station. The DSP provides address and data buses to receive / transmit digitized audio (via the DSP ASIC) and to access the DSP program and signal processing algorithms contained in three 32K x 8 SRAM ICs. It also provides a serial bus (SSI) to interface directly with linear Codec #1.

DSP ASIC

The DSP ASIC operates under control of the DSP to provide a number of functions, as follows:

- Interfaces with the DSP via the DSP address and data buses and interrupt request lines
- Accepts 16.8 MHz signal from Station Reference circuitry and outputs a 2.1 MHz reference signal used throughout the station, and a 1.2 MHz processor clock used by the MC68356 to generate the core clocks for the DSP and Host µP.
- Provides serial interfaces for linear Codec #5 and PCM codecs
- Provides serial interface for programming custom IC on Receiver Module, and accepts digitized data from custom IC via differential-to TTL converter circuitry
- Provides Receiver Signal Strength Indication (RSSI) data ouput

Audio Processing Circuitry

General

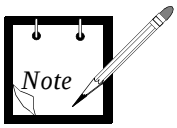
The Audio Processing circuitry interfaces external analog audio inputs and outputs with the DSP circuitry. The CLN1201 uses two linear codec ICs (referred to as Codec #1 and Codec #5) to handle wideband codec operation and the additional signal line requirements of trunking operation. Since audio signals input to or output from the DSP are in a digitized format, the codecs convert the audio signals between analog and digital formats as required.

Microphone and MRTI audio signals are digitized by Codec #2 (p/o Audio Processing Circuitry) before being sent to DSP ASIC via PCM Codec Bus

Speaker Audio

Speaker audio (to external speaker) is provided by codec #2. This signal is shared with MRTI RX Audio. The MRTI level is set (via the RSS) to suit MRTI output requirements. The adjustment is accomplished using a digital potentiometer which is controlled by the Host µP (via the SPI bus).

When the station is configured for operation with a full-duplex MRTI unit (the default is half-duplex), MRTI TX Audio is not routed to the speaker to prevent echo problems on the phone line. However, this also prevents use of the local microphone input and external speaker for MRTI testing.



Since trunking and MRTI share the same backplane connector, they are mutually exclusive.

Microphone

Microphone audio passes through preamp / bias generator circuitry to a switch which selects mic or MRTI TX Audio, and routes the result to Codec #2. A separate path from the preamp output routes mic audio to the MRTI RX Audio output. This allows mic audio to reach the MRTI output without appearing on the local speaker. Gain in the mic audio paths is chosen to match the required MRTI levels.

Discriminator Audio

DISC RX Audio is generated by linear Codec #5. Normally it is a wideband RX audio signal, available on the backplane for the system connector, the TCC connector (as Trunk RX Data), and for any option cards. However, it has three other functions as well:

- Under the influence of the Audio Mode input on the system connector, the signal is changed to band-limited RX audio with optional deemphasis and squelch.
- In line test mode, Line 1 input audio from the Wireline Interface Board (WIB) is routed to this output for level checking and test purposes.

Auxiliary TX Audio

The system connector input, Aux TX Audio, provides a path for audio from external equipment to reach the transmitter without passing through the wireline. The Audio Mode input switches it between wideband audio which is only splatter-filtered, and audio which is band-limited and preemphasized before being splatter-filtered. In either case, the audio reaches the DSP via codec #1. In line test mode, this input is routed to the Line 2 output for level setting and test purposes. In addition, for special applications, the signal can be routed directly to the exciter (i.e., does not pass through the DSP). There is no adjustable gain required for this input.

Wireline Interface Board Audio

Each of the wireline inputs / outputs has a programmable gain stage on the Wireline Interface Board (WIB). Digitized audio is carried to / from the DSP ASIC via the PCM Codec bus. When the line 1 / 2 pair carries narrow-band audio, the audio is converted to / from digital format by a PCM Codec on the WIB.

For the 8-wire model WIB, the line 3 / 4 pair are restricted to narrow-band audio, and are converted to / from digital format by a PCM Codec on the WIB.

MRTI Audio

MRTI audio is handled by Codec #2. In most installations, the MRTI is a half duplex device. This allows MRTI TX Audio to be routed to the local speaker (and thus to the MRTI RX AUDIO line) without causing echo problems (since the MRTI RX AUDIO line is muted in the MRTI). Gain in the MRTI paths is set by station software.

Full duplex MRTI operation is available, with the limitation that MRTI TX Audio does is not heard from the local speaker.

Trunking Audio

A trunking station can operate as either a control channel or a voice channel. In either case, wideband audio is routed to / from the Trunking Central Controller (TCC) as Trunk TX Data (through Codec #1) and Trunk RX Data (through Codec #5), providing paths for control and status tones. For voice channel operation, voice audio is routed to the WIB as described in the Wireline Audio section.

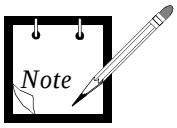
Exciter Modulation Signals

Digitized audio / data intended to be transmitted from the station is output from the DSP circuitry to Codec #1. The digitized signal is converted to analog, level shifted and amplified. The output is then fed to one of the inputs of a multiplexer switch. The output of the multiplexer is fed to two individual digitally-controlled potentiometers (each of which is adjusted by the Host µP via the SPI Bus) and output to the Exciter Module as modulation signals VCO MOD AUDIO and REF MOD AUDIO.

Parallel I/O Circuitry

General

The Parallel I/O circuitry allows the Host µP to generate SPI bus chip selects and to send/receive control signals to/from station modules and external options (via the backplane).



Refer to the Backplane section of this manual for complete details on the input/output signals which are routed to/from the backplane.

Input Circuitry

A buffer is provided to route serial station information (SERIAL ID IN) to the Host µP from a serial ID device on the station backplane.

An octal buffer is used to allow various input control signals from optional station circuitry (connected to the backplane) to be accepted and sent to the Host µP. This includes input signals from MRTI and trunking equipment.

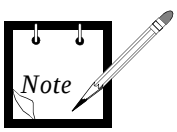
Output Circuitry

Two 1-of-16 demultiplexers are used to provide various SPI bus chip selects and four octal D flip-flops provide control signals to be output to the SCM, the Receiver and Exciter modules, and station circuitry (via the backplane). Control of the demultiplexers and flip-flops comes via the Host Data bus and associated chip select signals from the Host µP.

Front Panel LEDs

Four status LEDs are provided on the front panel to provide visual indications of various station operating conditions. The LEDs are driven, via software control, by five lines from an octal D flip-flop in the Parallel I/O circuitry.

The front panel **Station Status** indicator actually comprises two LEDs, one red and one green, which produce a bicolor effect to indicate different informational messages, depending on the particular LED(s) and duty cycle enabled. The resulting bicolor effect is achieved by locating the two LEDs adjacent to each other on the SCM board and combining the light sources through a single light pipe to the front panel.



Refer to the Station Operation section of this manual for complete details on the interpretation of the LEDs.

Supply Voltage Circuitry

The SCM contains on-board regulator and filtering circuitry to generate the various operating voltages required by the SCM circuitry. The SCM routes +10 V and +8 V from two regulators on the backplane to the Receiver and Exciter modules.

+14.2 V and +5V from the power supply (via the backplane) are used as sources for the following supply voltage circuits:

- +15 V Regulator Circuitry – voltage doubler circuit accepts +14.2 V input and feeds +15 V regulator to provide +15 V for the Receiver and Exciter modules.
- +12 V Regulator Circuitry – accepts input from the +15 V regulator to generate the voltage required (under Host μP control) for powering the Flash memory device during programming and erasing cycles.
- +5 V Regulator Circuitry – provides VCCA (analog +5 V) for the Audio Processing circuitry in the SCM.
- Filtering Circuitry – filters the +14.2 V and +5 V from the power supply (via backplane) to provide +14.2 V and VCC (digital +5 V) for the SCM digital circuitry.

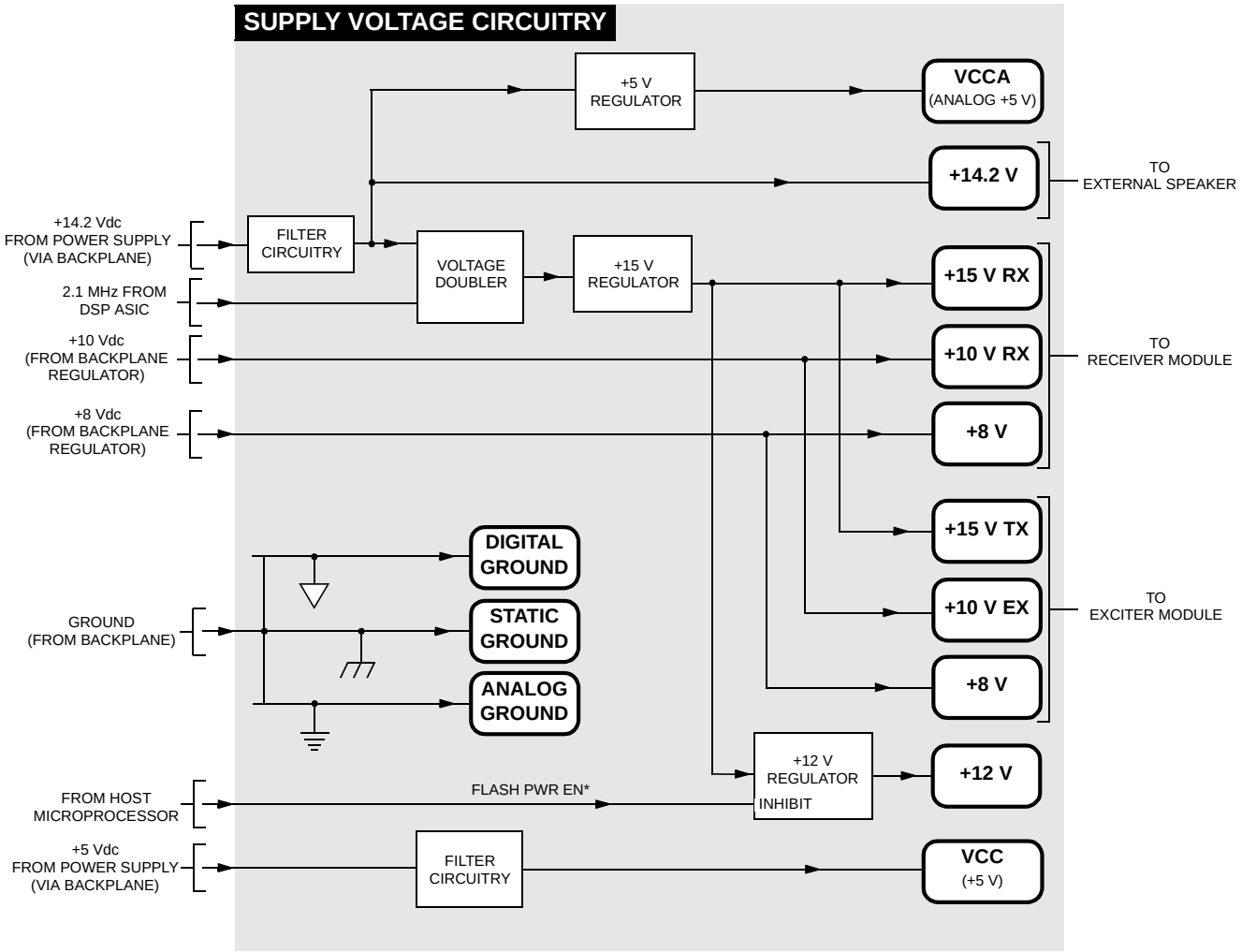


Figure 2. Station Control Module Functional Block Diagram - Supply Voltage Circuitry

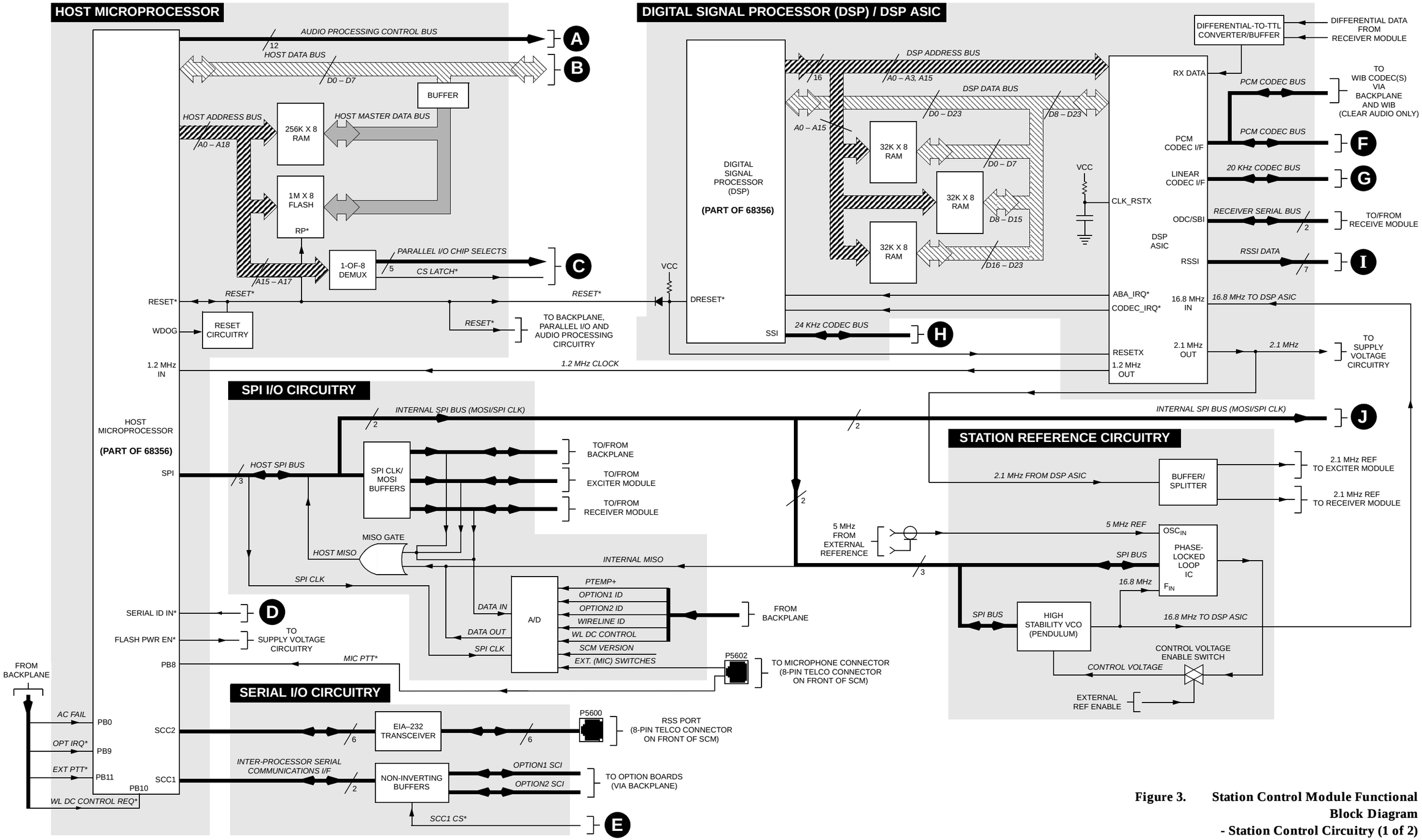


Figure 3. Station Control Module Functional Block Diagram - Station Control Circuitry (1 of 2)

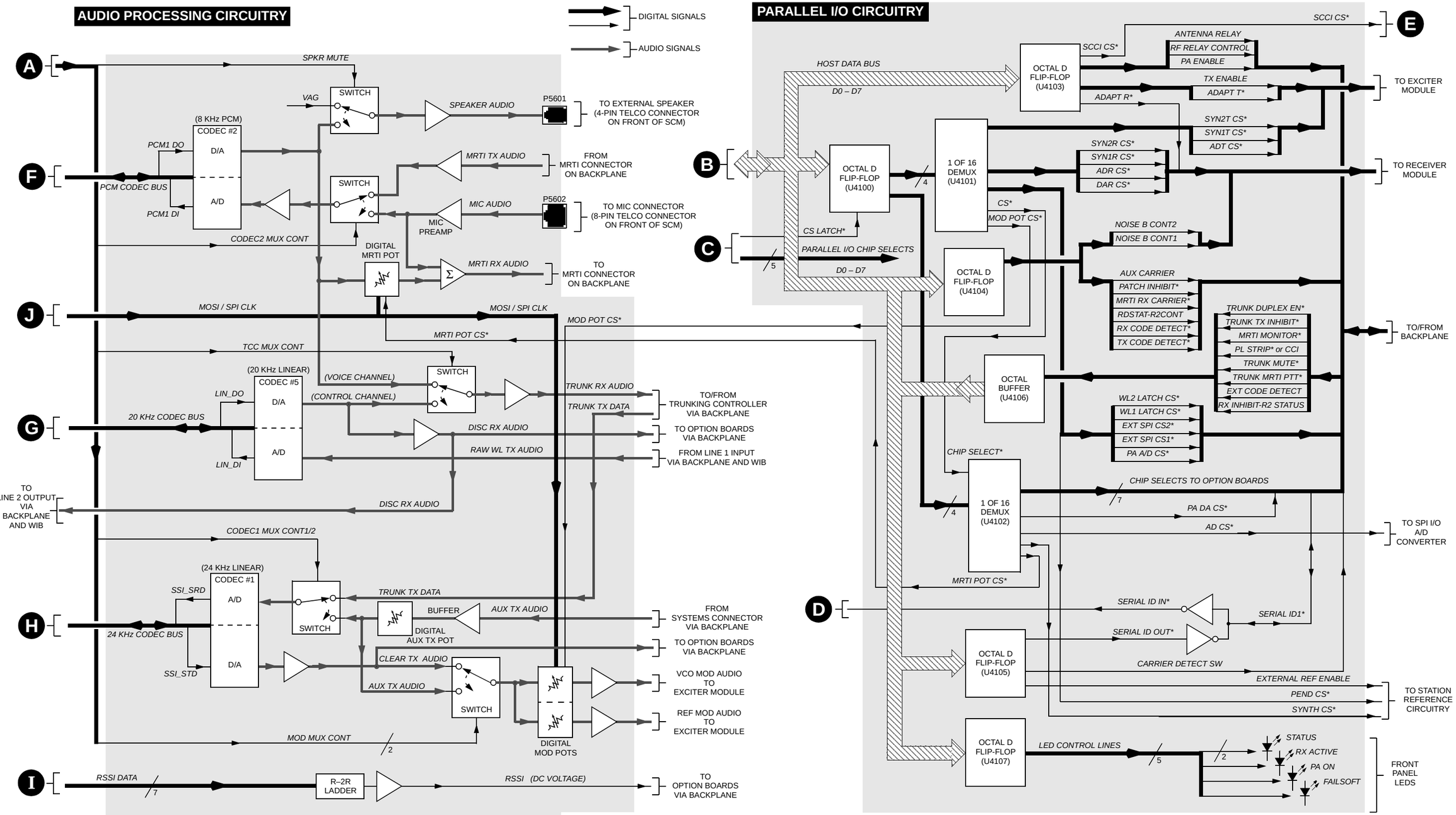


Figure 3. Station Control Module Functional Block Diagram - Station Control Circuitry (2 of 2)

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