MOTOROLA

BACKPLANE INTERCONNECT BOARD

MODEL CLN1202

1 DESCRIPTION

The CLN1202 Backplane Interconnect Board provides the electrical interconnections between the Station Control Module (SCM), the Power Supply, the Power Amplifier, and any optional plug-in modules of the station. The board also provides the connectors necessary to interface the station to phone lines, peripheral RF equipment, and other communications and maintenance equipment. This section provides a general description, identification of inputs / outputs, and a pin-out listing for all connectors, including information on signal names, functions, and levels.

General Description

The Backplane Interconnect Board (mounted across the rear of the station) is constructed with connectors on both sides. The connectors on one side mate with various station plug-in modules (such as the SCM, Wireline Interface Board and Auxiliary I / O option board); the connectors on the other side allow interface connections between the station and the phone lines, Power Supply, PA control signals, antenna relay, and other communications and maintenance equipment.

Commercial, Government, and Industrial Solutions Sector
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68P81096E46-E
12/20/98-UP

A metal shield mounts over the rear of the backplane board to provide protection for the circuit board runners and connector solder pads, ESD protection, and EMI / RFI shielding, as shown in Figure

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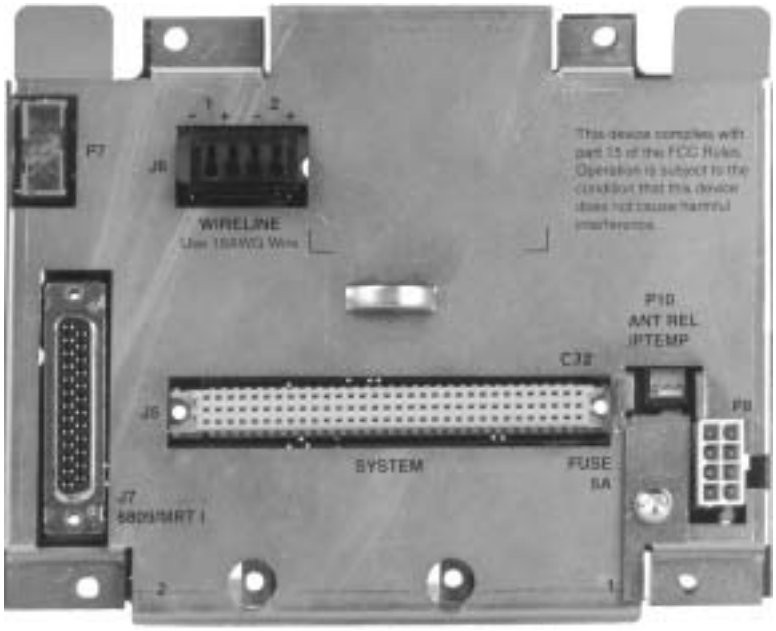


Figure 1. Backplane Interconnect Board

2 LOCATION OF BACKPLANE CONNECTORS

Figure 2 shows the location of the connectors on each side of the Backplane Interconnect Board.

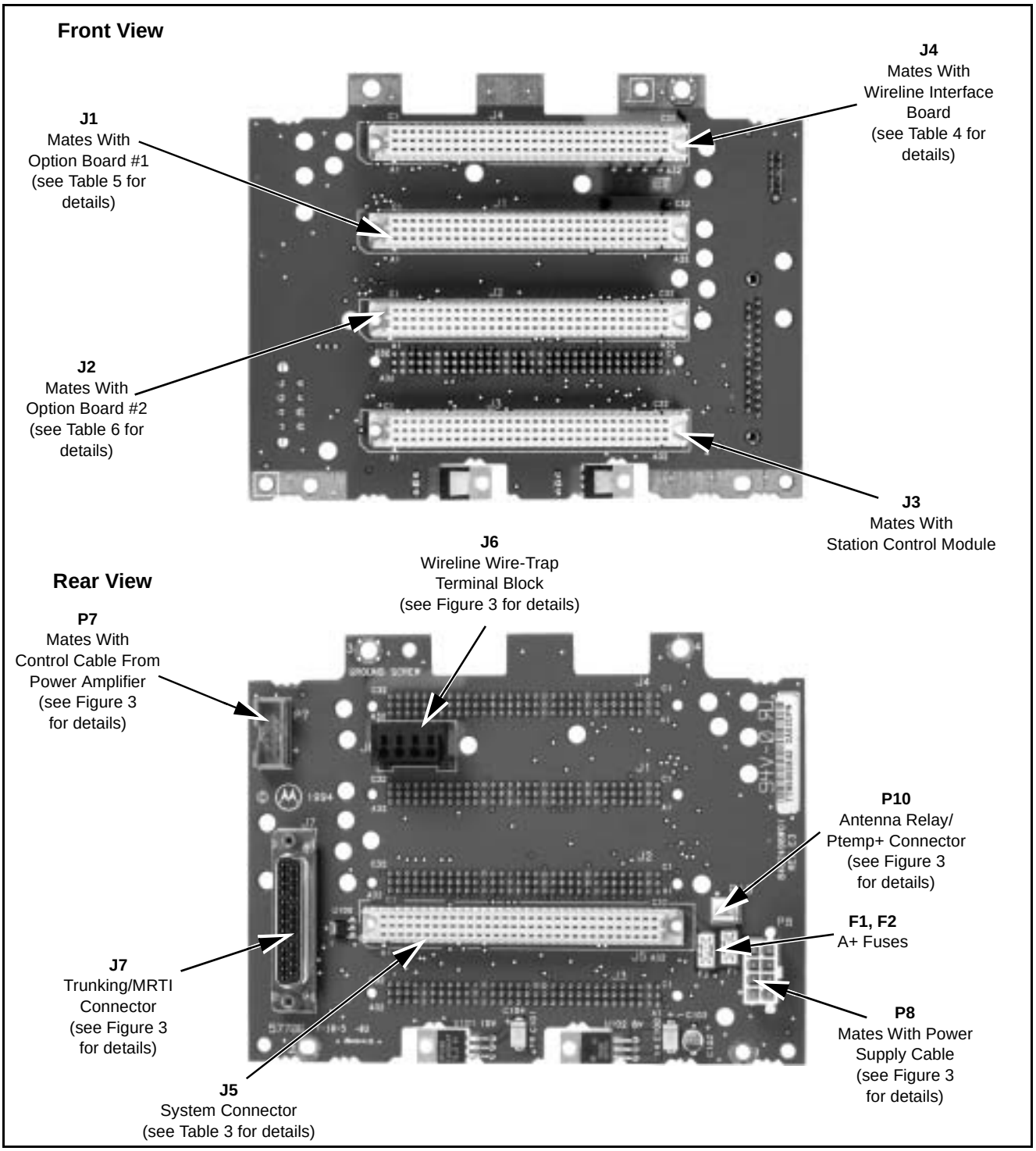


Figure 2. Station Backplane Connector Locations (Front and Rear Views)

3 BACKPLANE CONNECTORS INFORMATION

Each connector on the backplane has been assigned a connector designation number. For rear connectors, the connector number is stamped into the metal shield covering the rear of the backplane board. Labels for connectors which accept the plug-in modules are viewable when the front panel is removed. Table 1 lists each connector and its assigned designation number. Table 2 provides a detailed description of all of the backplane signals, arranged in alphanumeric order. NOTE: An asterisk (*) indicates an active low signal.

Figure 3 provides pin-out information for all non-Eurocard connectors located on the rear side of the backplane board. For the 96-pin Eurocard connectors, Tables 3 through 7 provide pinout information for each of these connectors. As shown, each connector pin is defined by signal name, input or output (with reference to connector), and the to/from location(s).

Table 1. Assigned Connector Number Vs. Function/Location Information

Connector	Function/Location
J1	96-pin Eurocard connector; accepts plug-in Option Board 1 (from front of station, behind front panel)
J2	96-pin Eurocard connector; accepts plug-in Option Board 2 (from front of station, behind front panel)
J3	96-pin Eurocard connector; accepts plug-in Station Control Module (from front of station, behind front panel)
J4	96-pin Eurocard connector; accepts plug-in Wireline Interface Board (from front of station, behind front panel)
J5	96-pin Eurocard connector; provides System connection to external communications equipment (on back of station)
J6	Wireline self-clamping terminals; accept customer phone line connections for 2-wire and 4-wire WIB configurations (on back of station) Note: This wire-trap terminal block accepts between .052 sq mm (20 AWG) and 0.2 sq mm (24AWG) solid wire or stranded wire. A stripped wire of any of these sizes can serve as a removable release tool.
J7	DB-25 connector; can be used for connection to trunking controller in wide-area trunking system, or to a Microprocessor Radio Telephone Interconnect (MRTI) (on back of station)
P7	10-pin connector; provides for connection to Power Amplifier (PA); routes SPI bus and chip selects from Station Control Module to PA (on back of station)
P8	8-pin connector; provides for connection to Power Supply module; routes dc supply voltages to station modules; routes AC Fail signal to Station Control Module (on back of station)
P10	Antenna Relay 3-pin connector; supplies control signals to antenna relay module; provides connection to a peripheral temperature sensing device such as found in an external circulator (on back of station)

Table 2. Backplane Signal Descriptions

Signal Name	Type	Function/Signal Levels
5 VDC	Power	+5 Vdc from Power Supply (1.5 Amp maximum)
8 VDC	Power	+8 Vdc from Regulator U102-3 (0.4 Amp maximum)
10 VDC EX	Power	+10 Vdc from U101-3 to Exciter Module via SCM (0.3 Amp maximum)
10 VDC RX	Power	+10 Vdc from U101-3 to Receiver Module via SCM (0.75 Amp maximum)
14.2 VDC	Power	+14.2 Vdc from Power Supply (8 Amp maximum from 500 W power supply; 16.5 Amp maximum from 250 W power supply)
28.6 VDC	Power	+28.6 Vdc from Power Supply directly to PA - 500 W power supply only (11.5 Amp maximum)
AC Fail	Digital	AC status signal from power supply to SCM; Active high indicates AC Mains failure
Antenna Relay	Digital	Open-collector control signal from SCM to antenna relay; Low to energize relay
Aux Carrier* or TSTAT	Digital	From SCM to MRTI (Aux Carrier*) to indicate RF channel activity (i.e. PA is keyed or second receiver is unsquelched); Active low (open-collector output)
		From SCM to TCC (“Transmitter Status”); Active high to indicate station is transmitting at rated power with an acceptable level of reflected power; low for any other condition; To opto-isolated input in TCC
Aux TX Audio	Analog	To SCM; Accepts wideband or voice-band audio from second receiver (selected by Aux TX Audio Mode (WCI)
Aux TX Audio Mode (WCI)	Digital	To SCM; Wild-Card Input selects mode of Disc RX Audio output & Aux TX Audio input
Carrier Detect Switch	Digital	From SCM to indicate carrier present; TTL active high
Carrier SQ Override (WCI)	Digital	Wild-Card Input disables carrier squelch gating qualifier; TTL active high
Chassis GND	Power	Station ground
Cntrl 14.2 VDC	Analog	+14.2 Vdc from Power Supply to Systems connector J5 (0.75 Amp maximum)
Coded WL RX Audio	Analog	Wideband (coded) audio to WIB; 5 Vdc maximum level
Disc RX Audio	Analog	Discriminator audio output from SCM; can be switched (by Aux TX Audio Mode) to be either buffered disc audio or de-emphasized RX audio (300 to 3 KHz)
Ext Code Detect	Digital	To SCM from external CIU; indicates code detect to reduce station turn-on delay; TTL active high
Ext Failsoft (WCI)	Digital	Wild-Card Input for wide-area trunking systems; TTL active high
Ext PTT*	Digital	Interrupt request to SCM to key transmitter; TTL active low
Ext Repeat* (WCI)	Digital	Wild-Card Input controls audio routing in wide-area trunking systems; TTL active low
Ext SPI CS1*	Digital	From SCM to Systems connector; SPI bus chip select; TTL active low
Ext SPI CS2*	Digital	From SCM to Systems connector; SPI bus chip select; TTL active low
Failsoft OUTPUT (WCO)	Digital	Wild-Card Output; active during failsoft to signal console in coded systems; TTL active low

Table 2. Backplane Signal Descriptions (Continued)

Signal Name	Type	Function/Signal Levels
GND	Power	Station ground
GPI_0 to GPI_15 (WCI)	Digital	General Purpose Inputs from external equipment (into the station at the System connector, through the Auxiliary I/O board, to the SCM).
GPO_0 to GPO_15 (WCO)	Digital	General Purpose Outputs to external equipment (from the SCM, through the Auxiliary I/O board, to the System connector).
GPIO_0 and GPIO_1	Digital	General Purpose Inputs and Outputs, to and from the SCM.
Line 1+	Analog	4-wire Phone Line (differential) inputs for clear audio and 12 kbps coded data; 300 to 3400 Hz (clear), or 30 to 6000 Hz (coded); 600Ω typical impedance (country-specific)
Line 1–		
Line 2+	Analog	2-wire Phone Line (differential) inputs/outputs or, 4-wire Phone Line outputs for clear audio and 12 kbps coded data; 300 to 3400 Hz (clear), or 30 to 6000 Hz (coded); 600Ω typical impedance (country-specific)
Line 2–		
Line 3+	Analog	Second Phone Line (differential) input pair for clear audio (8-wire WIB only); 300 to 3400 Hz; 600Ω typical impedance (country-specific)
Line 3–		
Line 4+	Analog	Second Phone Line (differential) output pair for clear audio (8-wire WIB only); 300 to 3400 Hz; 600Ω typical impedance (country-specific)
Line 4–		
MISO (Master In Slave Out)	Digital	SPI data from Slave devices to Master (SCM); standard TTL
MOSI (Master Out Slave In)	Digital	SPI data from Master (SCM) to Slave devices; standard TTL
MRTI RX Audio	Analog	From SCM; Station clear audio signals (RX, Wireline TX, or Mic) bound for landline via MRTI; MRTI accepts a 1.3 Vpp ±8 dB input level (MRTI has an ALC)
MRTI RX Carrier*	Digital	From SCM to MRTI to indicate squelch status of station and control direction of audio between SCM and MRTI for half-duplex patch modes (when signal is active, MRTI PTT is forced inactive and MRTI TX Audio is muted); Active during clear/coded reception and coded Repeater hang time, but *not* clear Repeater hang time; Also active for any PTT with higher priority than MRTI (i.e. normally active during Wireline PTT to force MRTI to mute MRTI TX Audio and instead route WL TX Audio to landline; Active low (open-collector output)
MRTI TX Audio	Analog	To SCM; MRTI audio from landline to be transmitted by station, or routed to WIB; Consists of subscriber signaling (i.e. selective signalling), call alert tones, and regular voice audio; Audio levels: either 80 mV_{rms} to 2 V_{rms} open circuit, or 15 mV_{rms} to 0.5 V_{rms} into 600Ω; Nominal level is 165 mV_{rms} for '#' tone pair into 600Ω (used to set 60% FSD)
OP1 CS1*	Digital	From SCM to Option 1 module; SPI bus chip selects; TTL active low
OP1 CS2*		
OP1 CS3*		
OP1 CS4*		
OP2 CS1*	Digital	From SCM to Option 2 module; SPI bus chip selects; TTL active low
OP2 CS2*		
OP2 CS3*		

Table 2. Backplane Signal Descriptions (Continued)

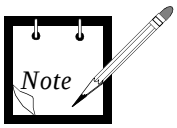
Signal Name	Type	Function/Signal Levels
Opt IRQ*	Digital	Interrupt request to SCM from Option cards; TTL active low
Option1 ID	Analog	Option 1 ID to SCM A/D; module ID determined by specific voltage; 0 to 5 Vdc
Option2 ID	Analog	Option 2 ID to SCM A/D; module ID determined by specific voltage; 0 to 5 Vdc
PA A/D CS*	Digital	From SCM; during SPI signalling, selects A/D converter in PA; TTL active low
PA D/A CS*	Digital	From SCM; during SPI signalling, selects D/A converter in PA; TTL active low
PA Enable*	Digital	From SCM; controls final module bias in low power PAs; TTL active low
PA Fail (WCO)	Digital	Auxiliary I/O board output indicates a PA failure; active high
PA Reset*	Digital	Resets D/A converter in PA; TTL active low (not used)
Patch Inhibit* or RSTAT	Digital	From SCM to MRTI to inhibit phone patch; Open-collector output (active low); While active, MRTI will not receive or place any calls
		From SCM to TCC to indicate receiver status; Open-collector output to opto-isolated input in TCC; Low when receiver is squelched, high when receiver is unsquelched
PL Detect Switch (WCO)	Digital	Wild-Card Output active when PL/DPL present; TTL active high
PL Strip* or CCI	Digital	Relay-closure input from MRTI to SCM (PL Strip*); Active low inhibits station TX PL; Typically used when MRTI transmits signalling information
		Logic input from TCC to provide Control Channel Indicate (CCI); Voice channel = high; Control channel = low; Driven by an opto-isolated open-collector with a Vce_{sat} of 1.0 V (maximum) @ a 2 mA load
Ptemp+	Analog	Input to SCM from peripheral temperature sensing device on circulator
Raw WL TX Audio	Analog	Wideband (coded) TX audio to SCM; 5 Vdc maximum level (if clipped)
Rdstat-R2 Control	Digital	From SCM to control second receiver; TTL active high
Repeater ON/OFF (WCI)	Digital	Wild-Card Input controls audio routing and repeater keyup; TTL
Reset*	Digital	System reset from SCM; TTL active low
RF Relay Control In	Digital	From SCM to control external RF relay driver; TTL active high
RF Relay Control Out	Relay Closure	From Auxiliary I/O to System connector to control external RF relay driver; TTL active high
RSSI	Analog	From SCM; DC voltage proportional to the receive RF signal strength; 0 to 5 Vdc
RX Inhibit-R2 Status	Digital	To SCM from second receiver to inhibit receiver audio to WIB
RX Lock (WCO)	Digital	Wild-Card Output indicates RX synthesizer is locked; TTL active high
RX PL Override (WCI)	Digital	Wild-Card Input disables PL gating qualifier; TTL active high
SCI RX Option1	Digital	To SCM from Option 1 card; for interprocessor communications; standard TTL
SCI RX Option2	Digital	To SCM from Option 2 card; for interprocessor communications; standard TTL
SCI TX Option1	Digital	From SCM to Option 1 card; for interprocessor communications; standard TTL

Table 2. Backplane Signal Descriptions (Continued)

Signal Name	Type	Function/Signal Levels
SCI TX Option2	Digital	From SCM to Option 2 card; for interprocessor communications; standard TTL
SpectraTac Enc Disable (WCI)	Digital	Wild-Card Input to disable SpectraTac status tone; TTL active high
Serial ID	Digital	Serial ID data to SCM from backplane serial ID device
SPI CLK	Digital	SCM SPI bus clock; Low-to-high transition shifts data; 310 KHz (minimum); standard TTL
Trunk Duplex Enable*	Digital	To SCM from TCC; active during full duplex phone calls to inhibit station repeat audio; TTL active low
Trunk /MRTI PTT*	Digital	To SCM from relay-closure (MRTI) or opto-isolated open-collector (TCC) to key transmitter; Active low
Trunk Mute*	Digital	Multi-purpose control signal to SCM from TCC; In some systems, active low mutes the repeat audio path and active high unmutes the audio path; Or, used by TCC to keep station out of failsoft by toggling this line periodically; Or, used to request a fast unmute of the Connect Tone (PL) decoder by receipt of a 1.6 ms pulse at start of voice calls; Driven by an opto-isolated open-collector with a Vce_{sat} of 1.0 V (maximum) @ a 2 mA load
Trunk RX Audio	Analog	Buffered RX discriminator audio sent to TCC; For control channels, it contains Inbound Signaling Words (ISW) (1.4 Vpp minimum, on a quiescent dc bias of 4.05 V ±1.5 Vdc); On voice channels, it contains connect and disconnect tones (0.7 to 2.0 Vpp, on a quiescent dc bias of 5 V ±0.25 Vdc), and high-speed acknowledge tones (2.5 to 6.0 Vpp, on a quiescent dc bias of 5 V ±0.25 Vdc)
Trunk TX Data+	Analog	Outbound TX modulation from TCC; Contains all trunking transmit data, including 3600 bps control channel data (8.8 Vpp ±0.4 V, 0 Vdc) and 300 or 150 bps voice channel data (2.8 Vpp ±0.3 V, 0 Vdc)
Trunk TX Data–	Analog	Trunking data signal ground
Trunk TX Inhibit*	Digital	To SCM; inhibits standby station; TTL active low
TX Lock (WCO)	Digital	Wild-Card Output indicates TX synthesizer is locked; TTL active high
TX PL On/Off (WCI)	Digital	Wild-Card Input To SCM; disables TX PL/DPL modulation; TTL active high
V Control	Analog	PA control voltage (P7 pin 4 only); 0 to 10 Vdc
Voltage Forward	Analog	DC voltage proportional to actual RF power output (P7 pin 1 only); 0 to 10 Vdc (Goes nowhere)
VSWR Fail*	Digital	VSWR falure indicated by active low.
Wireline 1/2 FSYNC	Codec	From SCM to WIB codec; 8 KHz frame sync clock initiates sampling of PCM transmit data output
Wireline 1/2 RXD	Codec	PCM receive data from SCM to WIB; standard TTL
Wireline 1/2 TXD	Codec	PCM transmit data from WIB; standard TTL
Wireline 3/4 FSYNC	Codec	From SCM to second WIB codec (8-wire WIB only); 8 KHz frame sync clock initiates sampling of PCM transmit data output
Wireline 3/4 RXD	Codec	PCM receive data to WIB (8-wire WIB only); standard TTL
Wireline 3/4 TXD	Codec	PCM transmit data from WIB (8-wire WIB only); standard TTL
Wireline BCLK	Codec	From SCM to WIB codec; 256 KHz (average) bit clock serially shifts data into/out of codec

Table 2. Backplane Signal Descriptions (Continued)

Signal Name	Type	Function/Signal Levels
Wireline ID	Analog	To SCM A / D from WIB; module ID determined by specific voltage; 0 to 5 Vdc
Wireline MCLK	Codec	From SCM to WIB codec; 256 KHz (average) master clock generates internal codec clock and sequencing signals; rising-edge aligned to frame sync clock
Wireline1 Latch CS*	Digital	Chip select for SPI latch on WIB; TTL active low
Wireline2 Latch CS*	Digital	Chip select for SPI latch #2 on 8-wire WIB only; TTL active low
WL DC Control	Analog	To SCM A / D from WIB which has DC remote control capability; voltage level corresponds to detected wireline current level
WL DC Control REQ*	Digital	Interrupt request to SCM from WIB which has DC remote control capability; TTL active low when control current detected on wireline



In Tables 3 to 7…

…the "To / From" column provides the source or destination of the signal as a connector number followed by a pin number. The first part (e.g. J3) represents the assigned connector number, followed by the specific connector pin number(s).

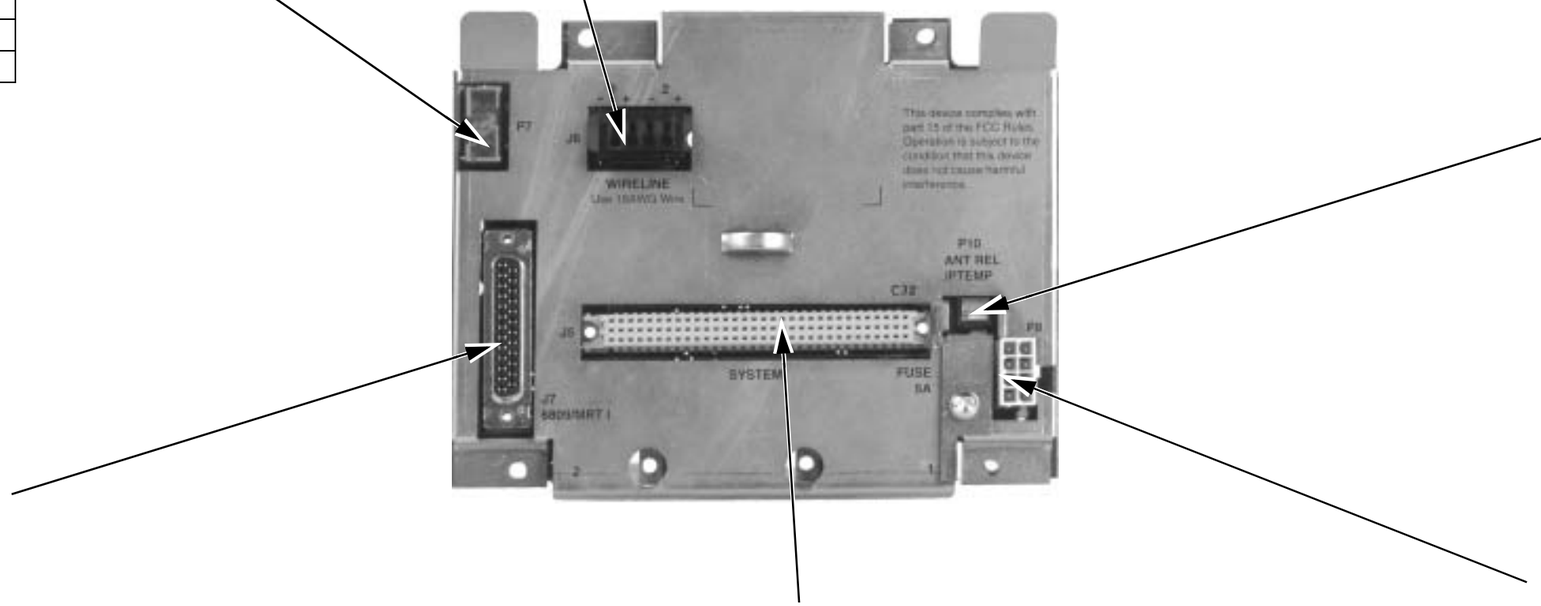
…symbols ′ and ″ indicate pin assignment functions which are jumper configurable. This applies to some General Purpose Inputs (GPIs) and some General Purpose Outputs (GPOs).

…an asterisk (*) indicates an active low signal.

P7 PA CONTROL CONNECTOR	
Pin No.	**Signal**
1	Voltage Forward
2	PA Enable*
3	PA Reset
4	V Control
5	GND
6	PA D / A CS*
7	SPI CLK
8	MOSI
9	MISO
10	PA A / D CS*

J6 WIRELINE TERMINALS	
Pin No.	**Signal**
1	Line 1– (Tx)
2	Line 1+ (Tx)
3	Line 2– (Rx)
4	Line 2+ (Rx)

J7 TRUNKING/MRTI CONNECTOR	
Pin No.	**Signal**
1	MRTI TX Audio
2	Trunk MRTI PTT*
3	Spare
4	MRTI Monitor*
5	Spare
6	Spare
7	MRTI RX Audio
8	Patch Inhibit* or RSTAT
9	GND
10	Aux Carrier* or TSTAT
11	Trunk MRTI PTT*
12	Aux Carrier* or TSTAT
13	Trunk TX Data+
14	Spare
15	MRTI RX Carrier*
16	GND
17	GND
18	GND
19	GND
20	Spare
21	Trunk TX Data–
22	Trunk RX Audio
23	Trunk Mute*
24	PL Strip* or CCI*
25	Patch Inhibit* or RSTAT



P10 ANTENNA RELAY / PTEMP+ CONNECTOR	
Pin No.	**Signal**
1	Antenna Relay
2	14.2 VDC
3	PTemp+

J5 SYSTEM CONNECTOR
See Table 3

P8 POWER SUPPLY CONNECTOR	
Pin No.	**Signal**
1	GND
2	GND
3	14.2 VDC
4	14.2 VDC
5	AC Fail
6	GND
7	5 VDC
8	5 VDC

The following symbols and abbreviations are used in Table 3:

- * = line is Active Low
- NS = Not Supported; **this pin should not be used**.
- Aux I / O = Indicates that the Aux I / O board must be present for this functionality.
- WCI = Wild Card Input
- WCO = Wild Card Output

Notes

The RSS Online Help provides the most current information on the System Connector pin assignments.

Figure 3. Backplane Rear Connector Pinout Information

Table 3. J5 SYSTEM CONNECTOR

Pin #	Row A	Input/ Output	To/From	Signal Characteristics	Row B	Input/ Output	To/From	Signal Characteristics	Row C	Input/ Output	To/From	Signal Characteristics
1	GPO_8 (WCO)	O	J1-C32, J2-C32	OCO, 100 mA, 40 V	RX Lock (Aux I/O)	O	J1-B32, J2-B32	OCO, 100 mA, 40 V; RX Lock, active high	TX Lock (Aux I/O)	O	J1-A32, J2-A32	OCO, 100 mA, 40 V; TX Lock, active high
2	PA Fail (Aux I/O)	O	J1-C31, J2-C31	OCO, 100 mA, 40 V, active low	GPO_13 (WCO)	O	J1-B31, J2-B31	OCO, 100 mA, 40 V	RdStat-R2 Control	O	J1-A31, J2-A31, J3-A26	TTL output, high when unsquelched
3	SCI_CLCK1	O	J1-C30, J2-C30, J3-C28	Do not use.	RdStat or GPO_15, Note 4	O	J1-B30, J2-B30	One side of relay closure, see C3	RdStat or GPO_15, Note 4	O	J1-A30, J2-A30	Other side of normally open relay, see B3
4	AC Fail	O	P8-5, J1-C29, J2-C29, J3-C24	TTL output, active high	Carrier Detect Switch	O	J1-B29, J2-B29, J3-B24	TTL output, active high	Failsoft Output (Aux I/O)	O	J1-A29, J2-A29	OCO, 100 mA, 40 V, active low
5	GPI_3 (WCI)	I	J1-C28, J2-C28	Pulled up transistor input, 16V max	GPI_8 (NS)	I	J1-B28, J2-B28	Pulled up transistor input, 16V max	GPI_4 (WCI)	I	J1-A28, J2-A28	Pulled up transistor input, 16V max
6	GP1_15 (–) (NS)	I	J1-C27, J2-C27	–ve side opto-isolated input, see C7	GPI_5 (NS)	I	J1-B27, J2-B27		Not Supported	I	J1-A27, J2-A27, J3-B26	
7	Ext Failsoft (Aux I/O)	I	J1-C26, J2-C26	Pulled up transistor input, 16V max	Ext Repeat* (Aux I/O)	I	J1-B26, J2-B26		GPI_15 (+) (NS)	I	J1-A26, J2-A26	+ve side opto-isolated input, see A6
8	GPI_1 (NS)	I	J1-C25, J2-C25		Trunk Duplex Enable*	I	J3-B25	TTL input	Trunk TX Inhibit*	I	J3-A25	TTL input
9	GPI_2 (NS)	I	J1-C24, J2-C24	Pulled up transistor input, 16V max	GPI_13 (WCI) or GPO_7 (NS)	I/O	J1-B24, J2-B24	Caution: See Auxiliary I/O section for jumpering information	RF Relay Control Out (Aux I/O)	O	J1-B5, J2-B5	OCO, 200 mA, 40 V, active high
10	VSWR_Fail* (Aux I/O)	O	J1-C23, J2-C23	Pulled up transistor output (10 kohms to +5 Vdc), active low	Spare 311	–	N/C		Ext PTT Out (Aux I/O) *, Note 5	I	J1-A23, J2-A23, J3-A23	TTL input
11	GPO_2 (WCO)	O	J1-C22, J2-C22	Pulled up transistor output (10 kohms to +5 Vdc)	GPI_12 (WCI) or GPO_6 (NS)	I/O	J1-B22, J2-B22	Caution: See Auxiliary I/O section for jumpering information	RSSI	O	J1-A22, J2-A22, J3-A22	RSS programmable sensitivity, Note 6
12	GPO_0 (WCO)	O	J1-B25, J2-B25		GPI_11 (WCI) or GPO_5 (NS)	I/O	J1-B23, J2-B23		GPI_10 (WCI) or GPO_4 (NS)	I/O	J1-A24, J2-A24	Caution: See Auxiliary I/O section for jumpering information
13	Antenna Relay	O	P10-1, J3-C26	OCO, 200 mA, active low	Spare 301	–	N/C		Spare 304	–	–	
14	Not Supported	O	J1-C18, J2-C18, J3-C19		Not Supported	I	J1-B19, J2-B19, J3-B19	TTL input	Not Supported	O	J1-A19, J2-A19, J3-A19	
15	Spare 310	–	–		GND	–	Station ground		GND	–	Station ground	
16	Spare 308	–	–		Spare 300	–	–		GND	–	Station ground	
17	Aux TX Audio	I	J1-C16, J2-C16, J3-C16	RSS programmable input sensitivity	Spare 321	–	–		Disc RX Audio	O	J1-A16, J2-A16, J3-A16	Discriminator audio, flat response; 80 mV to 400 mV for 60% deviation
18	Cntrl 14.2 VDC	O	P8 pins 3, 4 (thru F2)	+14.2 Vdc, Note 1	Cntrl 14.2 VDC	O	P8 pins 3, 4 (thru F2)	+14.2 Vdc, Note 1	Cntrl 14.2 VDC	O	P8 pins 3, 4 (thru F2)	+14.2 Vdc, Note 1
19	GND	–	Station ground		GND	–	Station ground		GND	–	Station ground	
20	5 VDC	O	P8 pins 7, 8	+5.1 ± 0.25 Vdc	5 VDC	O	P8 pins 7, 8	+5.1 ± 0.25 Vdc	5 VDC	O	P8 pins 7, 8	+5.1 ± 0.25 Vdc
21	Not Supported	O	J3-C12		RdStat or GPO_15, Note 4	O	J1-B12	OCO, 100 mA, 40 V	Not Supported	O	J3-A12	
22	GP1_7 (WCI)	I	J1-C11, J2-C11	Pulled up transistor input, 16V max.	Spare 322	–	–		Spare 302	–	–	
23	Spare 323	–	–		Spare 325	–	–		Spare 324	–	–	
24	Spare 320	–	–		Spare 309	–	–		GPIO_0 (CNTR I/O)	I/O	J1-A9, J2-A9, J3-A17	TTL input/output
25	Spare 903	–	–		Spare 902	–	–		Spare 317	–	–	
26	Ext PTT or GP1_14 (–), Note 1	I	J1-C7, J2-C7	–ve side opto-isolated input, see A29	Ext PTT or GPI_14, Note 2	I	J1-B7, J2-B7	Pulled up transistor input, 16V max, see A29	Spare 901	–	–	
27	GND	–	Station ground		GND	–	Station ground		GND	–	Station ground	
28	GPI_9 (WCI) or GPO_3 (NS)	I/O	J1-C6, J2-C6	Caution: See Auxiliary I/O section for jumpering information	Line 4+	O	J4-C10	Wireline output, balanced (+)	Line 3+	I	J4-C12	Wireline input, balanced (+)
29	Ext PTT or GPI_14 (–), Note 2	I	J1-C5, J2-C5	+ve. side opto-isolated input, see A26	AC Fail or GPO_14, Note 3	O	J1-B4, J2-B4	Other side of relay closure, see A30	GPIO_1 (CNTR I/O)	I/O	J1-A4, J2-A4, J3-A13	TTL input/output
30	AC Fail or GPO_14, Note 3	O	J1-C4, J2-C4	One side of normally open relay, see B29	Line 4–	O	J4-A9	Wireline output, balanced (–)	Line 3–	I	J4-A11	Wireline input, balanced (+)
31	GND	–	Station ground		GND	–	Station ground		GND	–	Station ground	
32	Cntrl 14.2 VDC	O	P8 pins 3, 4 (thru F2)	+14.2 Vdc, Note 1	Cntrl 14.2 VDC	O	P8 pins 3, 4 (thru F2)	+14.2 Vdc, Note 1	Cntrl 14.2 VDC	O	P8 pins 3, 4 (thru F2)	+14.2 Vdc, Note 1

Note 1: For dc-only 250 W power supplies, this voltage is equal to the input supply voltage.

Note 2: This pin can be jumpered for Ext PTT (supported) or GPI_14 (not supported). See Aux I/O jumpers P2 and P9.

Note 3: This pin can be jumpered for AC Fail (supported) or GPO_14 (not supported). See Aux I/O jumper P5.

Note 4: This pin can be jumpered for RdStat (supported) or GPO_15 (supported). See Aux I/O jumpers P3 and P4.

Note 5: Ext PTT signal output, taken from Ext PTT input. The output signal can be inverted, depending on jumper settings. See jumpers P2, P6, P9.

Note 6: For R03.01 (host software) and earlier, the fixed sensitivity is @ 172 mVrms for 60% system deviation. RSS programmable for pre-emphasized or flat response. DC offset +2.4 V. High impedance input.

Table 4. J4 WIRELINE CONNECTOR

Pin #	Row A	Input/Output	To/From	Row B	Input/Output	To/From	Row C	Input/Output	To/From
1	Wireline MCLK	I	J3-B6	Spare 5	–	–	Wireline BCLK	I	J3-C5
2	GND	–	Station ground	GND	–	Station ground	GND	–	Station ground
3	5 VDC	I	P8 pins 7, 8	5 VDC	I	P8 pins 7, 8	5 VDC	I	P8 pins 7, 8
4	GPIO_1 (CNTR I/O)	I/O	J1-A4, J2-A4, J5-C29, J3-A13	Wireline 3/4 TXD	O	J3-B4	Wireline 3/4 RXD	I	J3-C4
5	Wireline 1/2 TXD	O	J3-A5	Wireline 1/2 RXD	I	J3-B5	Spare 45	–	–
6	Wireline 3/4 FSYNC	I	J3-A6	Wireline2 Latch CS*	I	J3-B7	Wireline 1/2 FSYNC	I	J3-C6
7	MOSI	I	P7-8, J1-A7, J2-A7, J3-A7	Spare 18	–	–	Wireline1 Latch CS*	I	J3-C7
8	GND	–	Station ground	MISO	O	J1-B8, J2-B8, J3-B8, P7-9	SPI CLK	I	P7-7, J1-C8, J2-C8, J3-C8
9	Line 4–	O	J5-B30	GND	–	Station ground	GND	–	Station ground
10	Spare 28	–	–	Spare 37	–	–	Line 4+	O	J5-B28
11	Line 3–	I	J5-C30	Spare 19	–	–	Spare 10	–	–
12	Spare 1	–	–	Spare 38	–	–	Line 3+	I	J5-C28
13	WL DC Control	O	J3-A27	WL DC Control REQ*	O	J3-B27	Spare 46	–	–
14	GND	–	Station ground	GND	–	Station ground	GND	–	Station ground
15	14.2 VDC	I	P8 pins 3, 4 (thru F1)	14.2 VDC	I	P8 pins 3, 4 (thru F1)	14.2 VDC	I	P8 pins 3, 4 (thru F1)
16	Spare 2	–	–	Reset*	I	J1-B16, J2-B16, J3-B16, P7-3	Spare 47	–	–
17	Spare 29	–	–	Spare 6	–	–	Spare 24	–	–
18	Spare 15	–	–	Spare 20	–	–	Spare 25	–	–
19	Spare 30	–	–	Spare 39	–	–	Wireline ID	O	J3-C22
20	Spare 16	–	–	Coded WL RX Audio	I	J1-B20, J2-B20, J3-B20	Raw WL TX Audio	O	J1-C20, J2-C20, J3-C20
21	Chassis GND	–	–	Chassis GND	–	–	Chassis GND	–	–
22	Spare 31	–	–	Spare 40	–	–	Spare 27	–	–
23	Spare 3	–	–	Spare 7	–	–	Spare 11	–	–
24	Spare 32	–	–	Spare 41	–	–	Spare 48	–	–
25	Spare 17	–	–	Spare 21	–	–	Spare 49	–	–
26	Line 2+	I/O	J6-4	Line 2+	I/O	J6-4	Line 2+	I/O	J6-4
27	Spare 4	–	–	Spare 8	–	–	Spare 12	–	–
28	Line 2–	I/O	J6-3	Spare 22	–	–	Spare 50	–	–
29	Spare 34	–	–	Spare 43	–	–	Spare 26	–	–
30	Line 1+	I	J6- 2	Line 1+	I	J6-2	Line 1+	I	J6-2
31	Spare 36	–	–	Spare 23	–	–	Spare 51	–	–
32	Line 1–	I	J6-1	Spare 9	–	–	Spare 13	–	–

Table 5. J1 OPTION1 CONNECTOR

Pin No.	Row A	Input/ Output	To/From	Row B	Input/ Output	To/From	Row C	Input/ Output	To/From
1	Spare	–	–	Spare A12	–	J2-B1	Spare A1	–	–
2	GND	–	Station ground	GND	–	Station ground	GND	–	Station ground
3	5 VDC	I	P8 pins 7, 8	5 VDC	I	P8 pins 7, 8	5 VDC	I	P8 pins 7, 8
4	GPIO_1 (CNTR I/O)	I/O	J2-A4, J3-A13, J4-A4, J5-C29	GPO_14′ (WCO)	O	J2-B4, J5-B29	GPO_14 (WCO)	O	J2-C4, J3-A30
5	Spare	–	J2-A5	RF Relay Control Out	O	J2-B5, J5-C9	GPI_14′ (WCI)	I	J2-C5, J5-A29
6	Spare	–	J2-A6	RF Relay Control In	I	J2-B6, J3-A24	GPI_9 or GPO_3 (WCIO)	I/O	J2-C6, J5-A28
7	MOSI	I	P7-8, J2-A7, J3-A7, J4-A7	GPI_14 (WCI)	I	J2-B7, J5-B26	GPI_14′′ (WCI)	I	J2-C7, J5-A26
8	GND	–	Station ground	MISO	O	P7-9, J2-B8, J3-B8, J4-B8	SPI CLK	I	P7-7, J2-C8, J3-C8, J4-C8
9	GPIO_0 (CNTR I/O)	I/O	J2-A9, J3-A17, J5-C24	GND	–	Station ground	GND	–	Station ground
10	OP1 CS2*	I	J3-A10	OP1 CS4*	I	J3-B10	OP1 CS3*	I	J3-C10
11	Secure Control2	–	N/C	OP1 CS1*	I	J3-B11	GPI_7 (WCI)	I	J2-C11, J5-A22
12	SCI RX Option1	O	J3-A9	GPO_15′′ (WCO)	O	J5-B21	Spare A11	–	J2-C12
13	Spare	–	–	Spare A18	–	J2-B13	SCI TX Option1	I	J3-B9
14	GND	–	Station ground	GND	–	Station ground	GND	–	Station ground
15	14.2 VDC	I	P8 pins 3, 4 (thru F1)	14.2 VDC	I	P8 pins 3, 4 (thru F1)	14.2 VDC	I	P8 pins 3, 4 (thru F1)
16	Disc RX Audio	I	J2-A16, J3-A16, J5-C17	Reset*	I	J2-B16, J3-B16, J4-B16	Aux TX Audio	I	J2-C16, J3-C16, J5-A17
17	GND	–	Station ground	Decrypted RX Audio	I	J2-B17, J3-B17	Clear TX Audio	I	J2-C17, J3-C17
18	GND	–	Station ground	GND	–	Station ground	TX Code Detect*	I	J2-C18, J3-C19, J5-A14
19	RX Code Detect* (Future)	I	J2-A19, J3-A19, J5-C14	Ext Code Detect	I	J2-B19, J3-B19, J5-B14	Option1 ID	O	J3-C18
20	Coded Mod Audio	I	J2-A20, J3-A20	Coded WL RX Audio	I	J2-B20, J3-B20, J4-B20	Raw WL TX Audio	I	J2-C20, J3-C20, J4-C20
21	GND	–	Station ground	Secure RX Audio	I	J2-B21, J3-B21	GND	–	Station ground
22	RSSI	I	J2-A22, J3-A22, J5-C11	GPI_12 or GPO_6 (WCIO)	I/O	J2-B22, J5-B11	GPO_2 (WCO)	O	J2-C22, J5-A11
23	Ext PTT*	I	J2-A23, J3-A23, J5-C10	GPI_11 or GPO_5 (WCIO)	I/O	J2-B23, J5-B12	VSWR FAIL* (WCO)	O	J2-C23, J5-A10
24	GPI_10 or GPO_4 (WCIO)	I/O	J2-A24, J5-C12	GPI_13 or GPO_7 (WCIO)	I/O	J2-B24, J5-B9	GPI_2 (WCI)	I	J2-C24, J5-A9
25	Opt_IRQ*	O	J2-A25, J3-C23	GPO_0 (WCO)	O	J2-B25, J5-A12	GPI_1 (WCI)	I	J2-C25, J5-A8
26	GPI_15 (WCI)	I	J2-A26, J5-C7	Ext Repeat* (WCI)	I	J2-B26, J5-B7	Ext Failsoft (WCI)	I	J2-C26, J5-A7
27	RX Inhibit-R2 Status	I	J2-A27, J3-B26, J5-C6	GPI_5 (WCI)	I	J2-B27, J5-B6	GPI_15′ (WCI)	I	J2-C27, J5-A6
28	GPI_4 (WCI)	I	J2-A28, J5-C5	GPI_8 (WCI)	I	J2-B28, J5-B5	GPI_3 (WCI)	I	J2-C28, J5-A5
29	Failsoft OUTPUT (WCO)	O	J2-A29, J5-C4	Carrier Detect Switch	I	J2-B29, J3-B24, J5-B4	AC Fail	I	P8-5, J2-C29, J3-C24, J5-A4
30	GPO_15 (WCO)	O	J2-A30, J5-C3	GPO_15′ (WCO)	O	J2-B30, J5-B3	SCI_CLCK1	O	J2-C30, J5-A3, J3-C28
31	Rdstat-R2 Control	I	J2-A31, J5-C2, J3-A26	GPO_13 (WCO)	O	J2-B31, J5-B2	PA Fail (WCO)	O	J2-C31, J5-A2
32	TX Lock (WCO)	O	J2-A32, J5-C1	RX Lock (WCO)	O	J2-B32, J5-B1	GPO_8 (WCO)	O	J2-C32, J5-A1

Table 6. J2 OPTION2 CONNECTOR

Pin No.	Row A	Input/ Output	To/From	Row B	Input/ Output	To/From	Row C	Input/ Output	To/From
1	Spare A14	–	–	Spare A12	–	J1-B1	Spare A15	–	–
2	GND	–	Station ground	GND	–	Station ground	GND	–	Station ground
3	5 VDC	I	P8 pins 7, 8	5 VDC	I	P8 pins 7, 8	5 VDC	I	P8 pins 7, 8
4	GPIO_1 (CNTR I/O)	I/O	J1-A4, J3-A13, J4-A4, J5-C29	GPO_14′ (WCO)	O	J1-B4, J5-B29	GPO_14 (WCO)	O	J1-C4, J3-A3
5	Spare A16	–	J1-A5	RF Relay Control Out	O	J1-B5, J5-C9	GPI_14′ (WCI)	I	J1-C5, J5-A29
6	Spare A19	–	J1-A6	RF Relay Control In	I	J1-B6, J3-A24	GPI_19 or GPO_3 (WCIO)	I/O	J1-C6, J5-A28
7	MOSI	I	P7-8, J1-A7, J3-A7, J4-A7	GPI_14 (WCI)	I	J1-B7, J5-B26	GPI_14′′ (WCI)	I	J1-C7, J5-A26
8	GND	–	Station ground	MISO	O	P7-9, J1-B8, J3-B8, J4-B8	SPI CLK	I	P7-7, J1-C8, J3-C8, J4-C8
9	GPIO_0 (CNTR I/O)	I/O	J1-A9, J3-A17, J5-C24	GND	–	Station ground	GND	–	Station ground
10	OP2 CS2*	I	J3-A11	N/C	–	–	OP2 CS3*	I	J3-C11
11	Secure Control2	–	N/C	OP2 CS1*	I	J3-B12	GPI_7 (WCI)	I	J1-C11, J5-A22
12	SCI RX Option2	O	J3-C9	N/C	–	–	Spare A11	–	J1-C12
13	Spare A17	–	–	Spare A18	–	J1-B13	SCI TX Option2	I	J3-A8
14	GND	–	Station ground	GND	–	Station ground	GND	–	Station ground
15	14.2 VDC	I	P8 pins 3, 4 (thru F1)	14.2 VDC	I	P8 pins 3, 4 (thru F1)	14.2 VDC	I	P8 pins 3, 4 (thru F1)
16	Disc RX Audio	I	J1-A16, J3-A16, J5-C17	Reset*	–	J1-B16, J3-B16, J4-B16	Aux TX Audio	I	J1-C16, J3-C16, J5-A17
17	GND	–	Station ground	Decrypted RX Audio	I	J1-B17, J3-B17	Clear TX Audio	I	J1-C17, J3-C17
18	GND	–	Station ground	GND	–	Station ground	TX Code Detect*	I	J1-C18, J3-C18, J5-A14
19	RX Code Detect* (Future)	I	J1-A19, J3-A19, J5-C14	Ext Code Detect	I	J1-B19, J3-B19, J5-B14	Option2 ID	O	J3-B18
20	Coded Mod Audio	I	J1-A20, J3-A20	Coded WL RX Audio	I	J1-B20, J3-B20, J4-B20	Raw WL TX Audio	I	J1-C20, J3-C20, J4-C20
21	GND	–	Station ground	Secure RX Audio	I	J1-B21, J3-B21	GND	–	Station ground
22	RSSI	I	J1-A22, J3-A22, J5-C11	GPI_12 or GPO_6 (WCIO)	I/O	J1-B22, J5-B11	GPO_2 (WCO)	O	J1-C22, J5-A11
23	Ext PTT*	I	J1-A23, J3-A23, J5-C10	GPI_11 or GPO_5 (WCIO)	I/O	J1-B23, J5-B12	VSWR FAIL* (WCO)	O	J1-C23, J5-A10
24	GPI_10 or GPO_4 (WCIO)	I/O	J1-A24, J5-C12	GPI_13 or GPO_7 (WCIO)	I/O	J1-B24, J5-B9	GPI_2 (WCI)	I	J1-C24, J5-A9
25	OPT_IRQ*	O	J1-A25, J3-C23	GPO_0 (WCO)	O	J1-B25, J5-A12	GPI_1 (WCI)	I	J1-C25, J5-A8
26	GPI_15 (WCI)	I	J1-A26, J5-C7	Ext Repeat* (WCI)	I	J1-B26, J5-B7	Ext Failsoft (WCI)	I	J1-C26, J5-A7
27	RX Inhibit-R2 Status	I	J1-A27, J3-B26, J5-C6	GPI_5 (WCI)	I	J1-B27, J5-B6	GPI_15′ (WCI)	I	J1-C27, J5-A6
28	GPI_4 (WCI)	I	J1-A28, J5-C5	GPI_8 (WCI)	I	J1-B28, J5-B5	GPI_3 (WCI)	I	J1-C28, J5-A5
29	Failsoft OUTPUT (WCO)	O	J1-A29, J5-C4	Carrier Detect Switch	I	J1-B29, J3-B24, J5-B4	AC Fail	I	P8-5, J1-C29, J3-C24, J5-A4
30	GPO_15 (WCO)	O	J1-A30, J5-C3	GPO_15′ WCO)	O	J1-B30, J5-B3	SCI_CLCK1	O	J1-C30, J5-A3, J3-C28
31	Rdstat-R2 Control	I	J1-A31, J5-C2, J3-A26	PL Detect Switch (WCO)	O	J1-B31, J5-B2	PA Fail (WCO)	O	J1-C31, J5-A2
32	TX Lock (WCO)	O	J1-A32, J5-C1	RX Lock (WCO)	O	J1-B32, J5-B1	GPO_8 (WCO)	O	J2-C32, J5-A1

Table 7. J3 CONTROLLER CONNECTOR

Pin #	Row A	Input/Output	To/From	Row B	Input/Output	To/From	Row C	Input/Output	To/From
1	14.2 VDC	I	P8 pins 3, 4 (thru F1)	14.2 VDC	I	P8 pins 3, 4 (thru F1)	14.2 VDC	I	P8 pins 3, 4 (thru F1)
2	GND	–	Station ground	GND	–	Station ground	GND	–	Station ground
3	5 VDC	I	P8 pins 7, 8	5 VDC	I	P8 pins 7, 8	5 VDC	I	P8 pins 7, 8
4	8 VDC	I	U102-3	Wireline 3/4 TXD	I	J4-B4	Wireline 3/4 RXD	O	J4-C4
5	Wireline 1/2 TXD	I	J4-A5	Wireline 1/2 RXD	O	J4-B5	Wireline BCLK	O	J4-C1
6	Wireline 3/4 FSYNC	O	J4-A6	Wireline MCLK	O	J4-A1	Wireline 1/2 FSYNC	O	J4-C6
7	MOSI	O	P7-8, J1-A7, J2-A7, J4-A7	Wireline2 Latch CS*	O	J4-B6	Wireline1 Latch CS*	O	J4-C7
8	SCI TX Option2	O	J2-C13	MISO	I	P7-9, J1-B8, J2-B8, J4-B8	SPI CLK	O	P7-7, J1-C8, J2-C8, J4-C8
9	SCI RX Option1	I	J1-A12	SCI TX Option1	O	J1-C13	SCI RX Option2	I	J2-A12
10	OP1 CS2*	O	J1-A10	OP1 CS4*	O	J1-B10	OP1 CS3*	O	J1-C10
11	OP2 CS2*	O	J2-A10	OP1 CS1*	O	J1-B11	OP2 CS3*	O	J2-C10
12	Ext SPI CS1*	O	J5-C21	OP2 CS1*	O	J2-B11	Ext SPI CS2*	O	J5-A21
13	GPIO_1 (CNTR I/O)	I/O	J1-A4, J2-A4, J5-C29	PA D/A CS*	O	P7-6	PA A/D CS*	O	P7-10
14	10 VDC EX	I	Regulator U101-3	10 VDC EX	I	Regulator U101-3	GND	–	Station ground
15	10 VDC RX	I	Regulator U101-3	10 VDC RX	I	Regulator U101-3	GND	–	Station ground
16	Disc RX Audio	O	J1-A16, J2-A16, J5-C17	Reset*	O	J1-B16, J2-B16, J4-B16, P7-3	Aux TX Audio	I	J1-C16, J2-C16, J5-A17
17	GPIO_0 (CNTR I/O)	I/O	J1-A9, J2-A9, J5-C24	Decrypted RX Audio	I	J1-B17, J2-B17	Clear TX Audio	O	J1-C17, J2-C17
18	Ptemp+	I	P10-3	Option2 ID	I	J2-C19	Option1 ID	I	J1-C19
19	RX Code Detect*	O	J1-A19, J2-A19, J5-C14	Ext Code Detect	I	J1-B19, J2-B19, J5-B14	TX Code Detect*	O	J1-C18, J2-C18, J5-A14
20	Coded Mod Audio	I	J1-A20, J2-A20	Coded WL RX Audio	O	J1-B20, J2-B20, J4-B20	Raw WL TX Audio	I	J1-C20, J2-C20, J4-C20
21	GND	–	Station ground	Secure RX Audio	I	J1-B21, J2-B21	GND	–	Station ground
22	RSSI	O	J1-A22, J2-A22, J5-C11	GND	–	Station ground	Wireline ID	I	J4-C19
23	Ext PTT*	I	J1-A23, J2-A23, J5-C10	N/C	–		Opt IRQ*	O	J1-A25, J2-A25
24	RF Relay Control	O	J1-B6, J2-B6	Carrier Detect Switch	O	J1-B29, J2-B29, J5-B4	AC Fail	I	P8-5, J1-C29, J2-C29, J5-A4
25	Trunk TX Inhibit*	I	J5-C8	Trunk Duplex Enable*	I	J5-B8	Serial ID	I	U100-2
26	Rdstat-R2 Control	O	J1-A31, J2-A31, J5-C2	RX Inhibit-R2 Status	I	J1-A27, J2-A27, J5-C6	Antenna Relay	O	P10-1, J5-A13
27	WL DC Control	I	J4-A13	WL DC Control REQ*	I	J4-B13	PA Enable*	O	P7-2
28	GND	–	Station ground	GND	–	Station ground	SCI_CLCK1	O	J1-C30, J5-A3, J2-C30
29	Trunk RX Audio	O	J7-22	Trunk TX Data+	I	J7-13	Trunk TX Data–	I	J7-21
30	MRTI RX Audio	O	J7-7	MRTI TX Audio	I	J7-1	Aux Carrier* or TSTAT	O	J7-12, J7-10
31	Trunk Mute*	I	J7-23	MRTI RX Carrier*	O	J7-15	PL Strip* or CCI	I	J7-24
32	Patch Inhibit* or RSTAT	O	J7-25	MRTI Monitor*	I	J7-4	Trunk MRTI PTT*	I	J7-2, J7-11